

This exam will be conducted according to the Georgia Tech Honor Code. I pledge to neither give nor receive unauthorized assistance on this exam and to abide by all provisions of the Honor Code.

Signed (With your Full Legal Name):

SOLUTION

Instructions: Instructions: This is a closed book, closed note exam. Calculators are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.

Good Luck!

Your Name (please print): _____

For maximum (and partial) credit, show your work.

Good Luck!

1	2	3	4	5	total
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20	20	20	20	20	100

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Problem 1 (5 parts, 20 points)

Fundamentals

Part A (12 points) Convert the following notations using the minimum required number of digits.

Binary Notation	Decimal Notation
100011	35
10111	23

Binary Notation	Octal Notation	Hexadecimal Notation
10110011	263	B3
1000010	102	42

Part B (2 points) Which one of the following fundamental Boolean algebra operators performs a logical multiplication?

- a) NOT
- b) **AND**
- c) OR
- d) XOR

Part C (2 points) The duality principle states that any theorem or identity in Boolean algebra is also true if 0s and 1s and then AND and OR operators are swapped throughout.

- a) **True**
- b) False

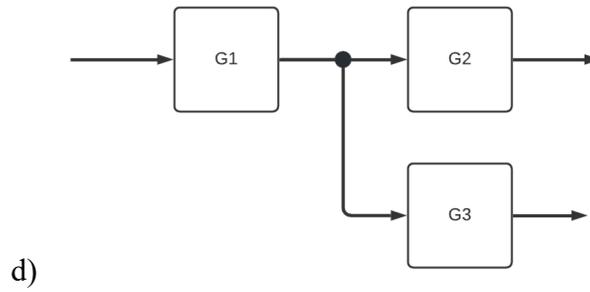
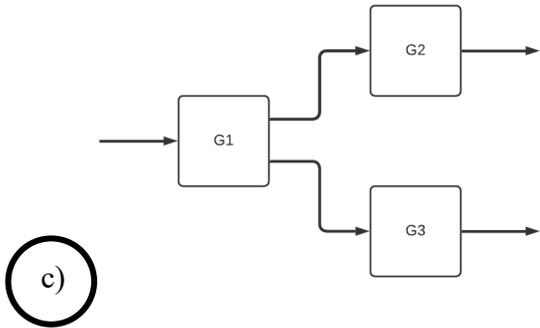
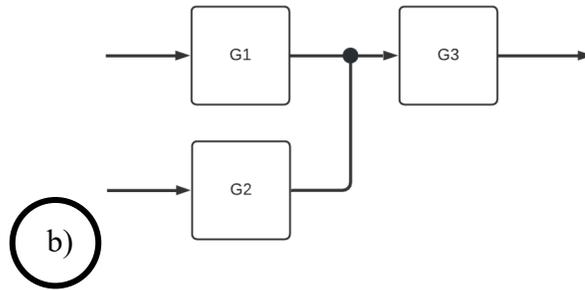
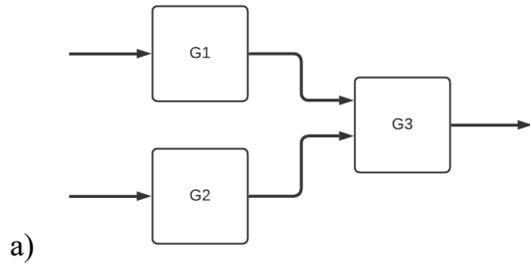
Part D (2 points) Which one of the following statements about CMOS transistor switches is **NOT** true?

- a) Two ideal switches connected in series implement the AND operator.
- b) nMOS transistors transmit logic level 0 well and logic level 1 poorly when CLOSED.
- c) **High impedance is a state where a transistor switch is CLOSED.**
- d) The impedance of a transistor switch is on the order of 100MΩ when it is OPEN.

Problem 1 Cont. (5 parts, 20 points)

Fundamentals

Part E (2 points) Which of the following networks is invalid? Circle all that apply.



Problem 2 (2 parts, 20 points)

Boolean Algebra

Part A (12 points) Transform the following Boolean expression to a form where it is ready for switch-level implementation. In other words, convert it to a format where there are complement bars over only input variables, not over operations. The behavior of the expression should remain unchanged. **Do not implement.**

$$\text{Out}_{A1} = \overline{\overline{\overline{A + B} \cdot \overline{C + D}}}$$

$$\text{Out}_{A1} = \overline{A} + B + C + D$$

$$\text{Out}_{A2} = \overline{(\overline{A + B}) + (\overline{C \cdot (D + \overline{E})}) \cdot \overline{F} \cdot G}$$

$$\text{Out}_{A2} = (A \cdot \overline{B}) + (C + \overline{(D + \overline{E})}) \cdot F + \overline{G}$$

$$\text{Out}_{A2} = \overline{(\overline{A + B}) \cdot (\overline{C \cdot (D + \overline{E})}) \cdot \overline{F} \cdot G}$$

$$\text{Out}_{A2} = (A \cdot \overline{B}) + (C + \overline{D} \cdot E) \cdot F + \overline{G}$$

Part B (8 points) Given the Boolean algebra equation: $\text{Out}_B(A, B, C) = B\overline{C} + A\overline{B} + \overline{A}BC$

a) (4 points) Give the truth table for Out_B .

A	B	C	Out_B
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

b) (2 points) Give the canonical **product of sums (POS) Boolean representation** for Out_B .

$$\text{Out}_B = (A + B + C)(A + B + \overline{C})(\overline{A} + \overline{B} + \overline{C})$$

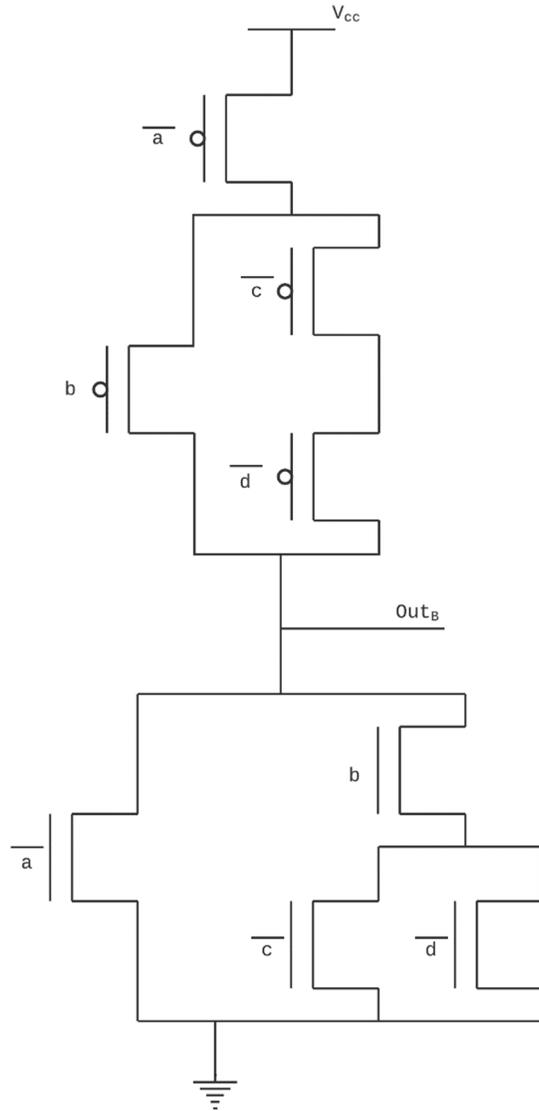
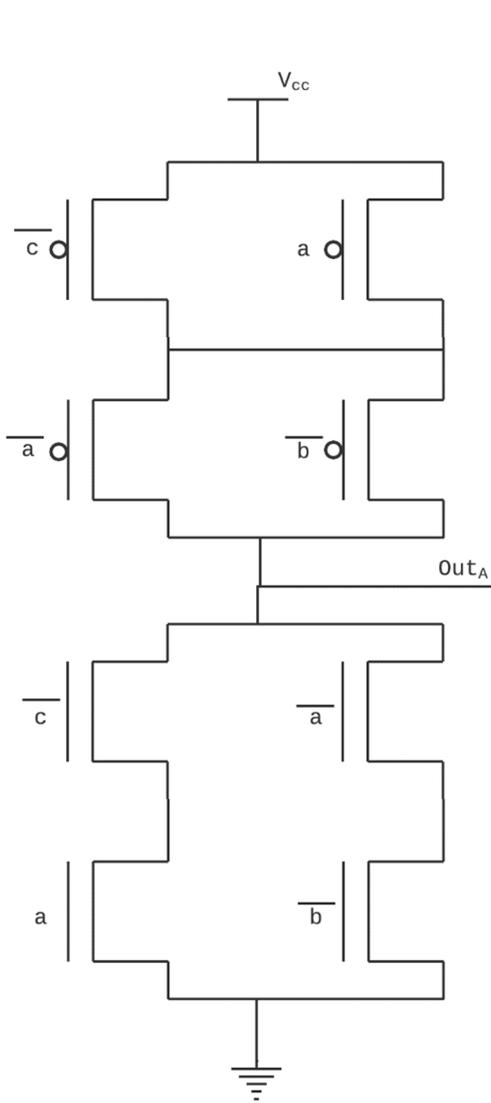
c) (2 points) Give the **canonical sum of minterms ($\sum(i)$) representation** for Out_B .

$$\text{Out}_B = \sum m(2,3,4,5,6)$$

Problem 3 (4 parts, 20 points)

Switched Networks

For each partial switch network below, draw the missing pull-up or pull-down network so that the circuit contains no floats or shorts. Assume both inputs and their complements are available. Also, write the Boolean expression computed by the completed circuit. (The expression should have complements only over the individual input signals, not over subexpressions.) Do not simplify the equations.

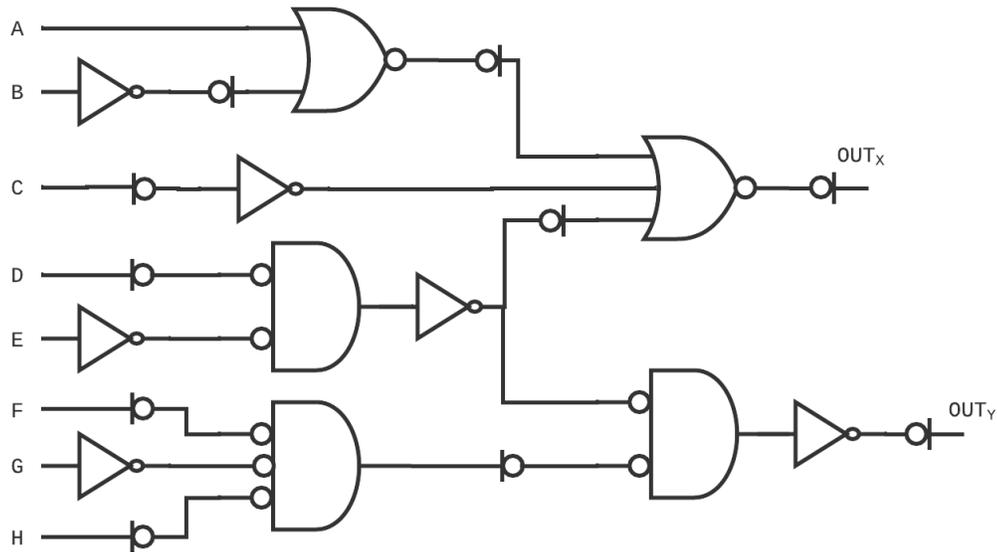


Out_A = $(\bar{c} + \bar{a}) \cdot (a + b)$

Out_B = $a \cdot (\bar{b} + \bar{c} \cdot \bar{d})$

Problem 4 (2 parts, 20 points)

Mixed Logic Reengineering



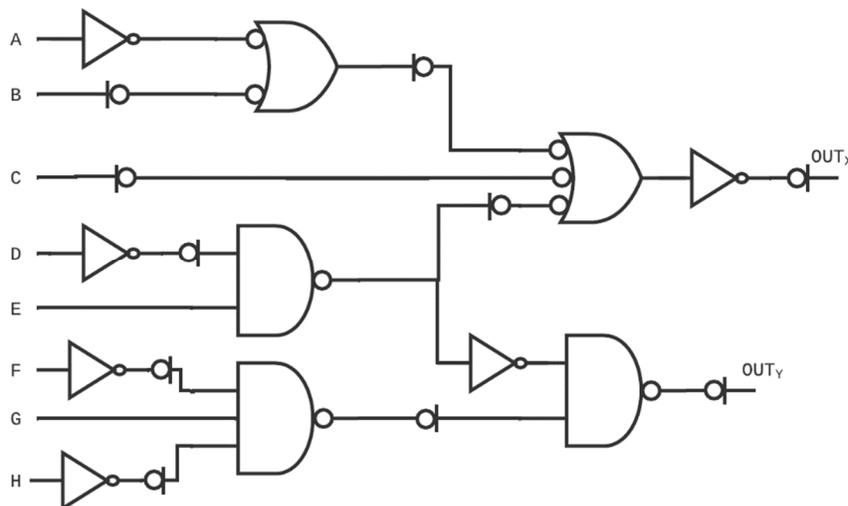
Part A (10 points) Write the output expression for the gate design shown above. Also determine the number of transistors used in its implementation.

$$Out_X = \overline{\overline{A + \overline{B} + \overline{C} + \overline{D} \cdot E}}$$

$$Out_Y = \overline{\overline{D \cdot E \cdot (\overline{F \cdot G \cdot H})}}$$

$$\# \text{ transistors} = 2 \times 6T + 3 \times 4T + 6 \times 2T = 36 \text{ transistors}$$

Part B (10 points) Now reimplement these expressions using NAND gates and inverters. Determine the number of transistors used in this implementation.



$$\# \text{ transistors} = 2 \times 6T + 3 \times 4T + 6 \times 2T = 36 \text{ transistors}$$

Problem 5 (2 parts, 20 points)

Karnaugh Maps

Part A (10 points) Simplify the following product-of-sums (POS) expression using a Karnaugh Map. Circle and list all prime implicants, indicating which are essential, and write the *sum-of-products* (SOP) expression.

$$F(A, B, C, D) = \prod (4,5,6,10,11,14,15)$$

		CD			
	AB	00	01	11	10
00		1	1	1	1
01				1	
11		1	1		
10		1	1		

Prime Implicants:

1. BC

2. AC

3. A \bar{B}

4. $\bar{A}CD$

5. _____

6. _____

7. _____

Essential?

Y or N?

Y or N?

Y or N?

Y or N?

Y or N?

Y or N?

Y or N?

Simplified SOP expression $F(A, B, C, D) = AC + \bar{A}\bar{B} + \bar{A}CD$

Part B (10 points) Given the following Karnaugh Map, circle and list all the prime implicants, indicating which are essential and write the simplified *product-of-sums* (POS) expression.

		CD			
	AB	00	01	11	10
00		1	0	0	1
01		1	X	X	1
11		1	0	0	0
10		X	0	0	0

Prime Implicants:

1. \bar{D}

2. $\bar{A} + \bar{C}$

3. _____

4. _____

5. _____

6. _____

7. _____

Essential?

Y or N?

Simplified POS expression $\bar{D} \cdot (\bar{A} + \bar{C})$