

**Problem 1** (3 parts, 30 points)**Memory Chips/Systems**

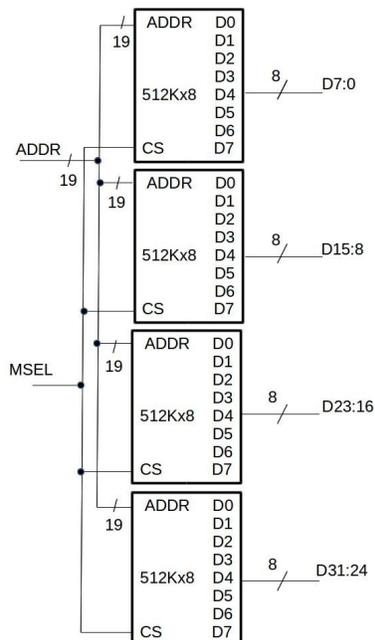
**Part A** (12 points) Consider a **512 MByte** DRAM chip organized as **128 million addresses** of **32-bit words**. Assume both the DRAM cell and the DRAM chip are square. The column number and offset concatenate to form the memory address. Using the organization approach discussed in class, answer the following questions about the chip. *Express all answers in decimal (not powers of two).* 1byte = 8 bits.

|  |   |
|--|---|
| total number of bits in address          | <u>27 bits</u>  |
| number of columns                        | <u><math>\sqrt{2^{32}} = 2^{16} = 64\text{K}</math></u> |
| column decoder required ( $n$ to $m$ )   | <u>16 to 64K</u>  |
| number of words per column               | <u><math>2^{16}/2^5 = 2^{11} = 2\text{K}</math></u>     |
| type of mux required ( $n$ to $m$ )      | <u>2K to 1</u>  |
| number of address lines in column offset | <u>11</u>   |

**Part B** (10 points) Consider an **128 MByte** memory system with **8 million addresses** of **16 byte words** using a **2 million** address by **16-bit word** memory DRAM chip.

|   |   |
|---|---|
| <b>word</b> address lines for memory system | <u>23</u>   |
| chips needed in one bank                    | <u><math>2^4 \cdot 2^3 / 2^4 = 2^3 = 8</math></u> |
| banks for memory system                     | <u>8/2 = 4</u>                                    |
| memory decoder required ( $n$ to $m$ )      | <u>2 to 4</u>                                     |
| DRAM chips required                         | <u>8*4 = 32</u>                                   |

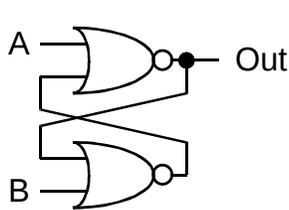
**Part C** (8 points) Design a **512K address by 4 byte** memory system with **512K address by 8-bit** memory chips. *Label all busses and indicate bit width.* Assume R/W is connected and not shown here. Use a bank decoder if necessary. Be sure to include the address bus, data bus, and MSEL.



**Problem 2** (3 parts, 30 points)

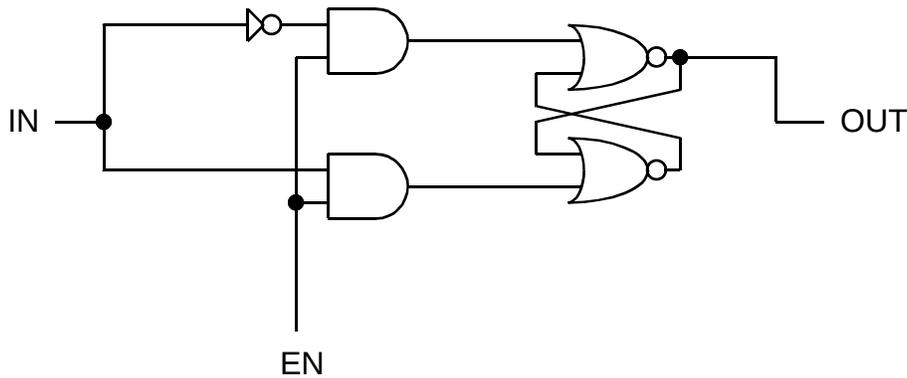
**Latches**

**Part A** (12 points) For the circuit below, complete the truth table describing its behavior. Then label the status of each row from the following choices: SET, RESET, HOLD, DISALLOWED.

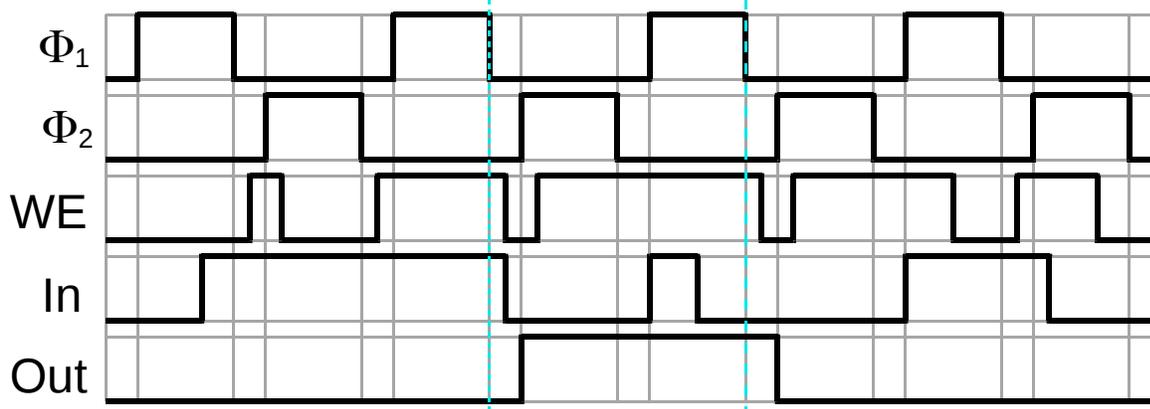


| A | B | Out   | status     |
|---|---|-------|------------|
| 0 | 0 | $Q_0$ | HOLD       |
| 1 | 0 | 0     | RESET      |
| 0 | 1 | 1     | SET        |
| 1 | 1 | 0     | DISALLOWED |

**Part B** (9 points) Now implement a transparent latch using this circuit plus additional basic gates (AND, OR, NAND, NOR, and NOT). Label inputs IN and EN. Label output OUT. Do **not** attempt to employ mixed logic notation.



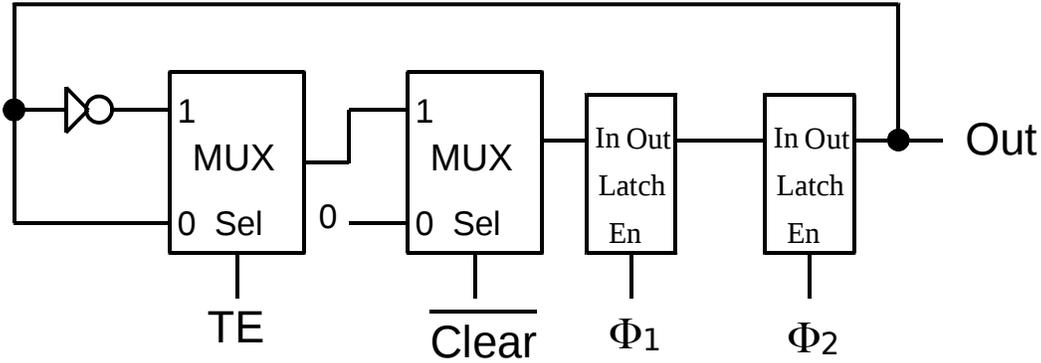
**Part C** (9 points) Assume the following signals are applied to a register with write enable. Draw the output signal **Out**. Draw a vertical line where **In** is sampled. Assume **Out** starts at zero.



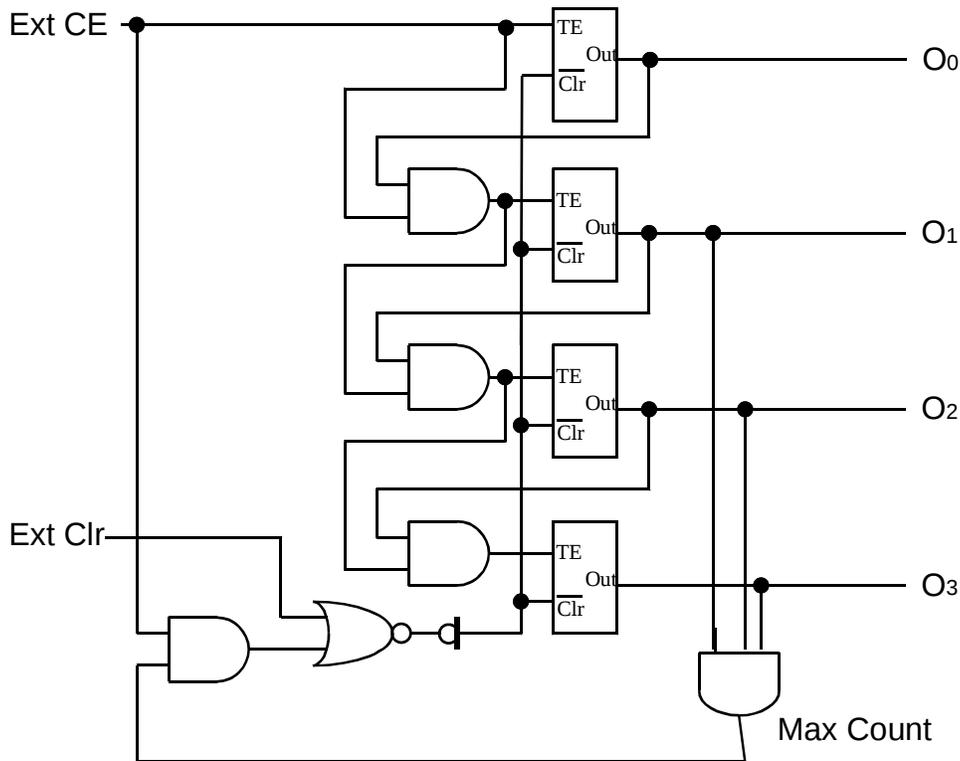
**Problem 3** (2 parts, 15 points)

**Counter Design**

**Part A** (7 points) Design a toggle cell using *only* transparent latches, inverters, and 2-to-1 multiplexers (*no basic gates besides inverters*). Use icons for the latches and muxes. Your toggle cell should have an active high toggle enable input **TE**, and an active low clear input  $\overline{\text{Clear}}$ , two-phase non-overlapping clock inputs  $\Phi_1$  and  $\Phi_2$ , and a single output **Out**. The  $\overline{\text{Clear}}$  signal has precedence over **TE**. *Label all signals.*



**Part B** (8 points) Consider the following incomplete counter. Based on the completed Max Count detector, determine and describe the counter type. Then complete the counter by properly generating the active low  $\overline{\text{Clr}}$  signal when either the external clear is asserted or the counter is about to exceed the maximum count. Use any basic gates required.



It's a divide by 15 counter.

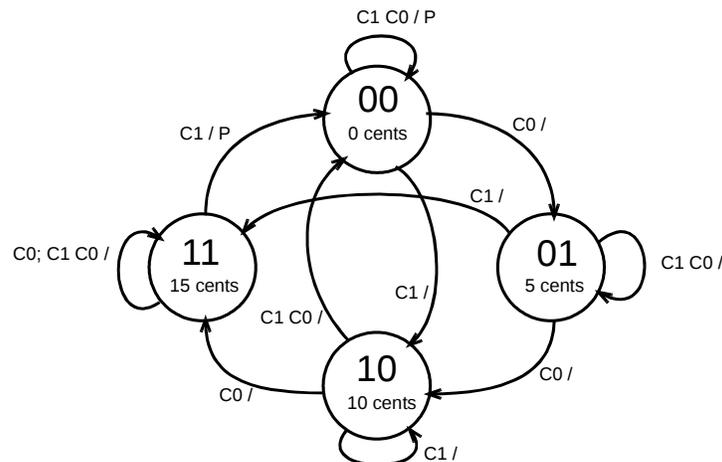
**Problem 4** (3 parts, 25 points)

**State Machines**

A state diagram for the controller of the StickyFinger snack machine is shown below. The machine accepts nickels, dimes, and quarters, and does not give change. It sometimes dispenses a bag of pretzels when coins are inserted. Slugs are not detected. The inputs to the controller are C1 and C0, which indicate which coin is inserted according to the following table.

| coin inserted | C1 | C0 |
|---------------|----|----|
| nickel        | 0  | 1  |
| dime          | 1  | 0  |
| quarter       | 1  | 1  |

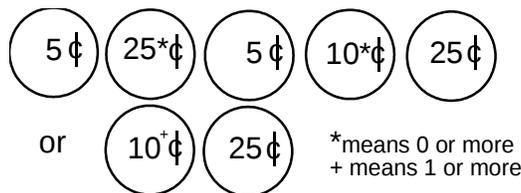
When the P output signal is asserted, a snack bag of pretzels is dispensed. The states keep track of how much money the machine “believes” you have inserted so far. They are number 00 for zero cents, 01 for five cents, 10 for ten cents, 11 for fifteen cents. Unfortunately, as you can see from the state diagram, the machine is not always accurate in keeping track of the money you have inserted.



**Part A** (5 points) Determine the minimum cost of a bag of pretzels.

Pretzels cost a minimum of 25 cents.

**Part B** (8 points) The machine occasionally keeps your money without giving you pretzels. Give an example of a sequence of coins where you would end up in the 0 cents state (00) and not get any pretzels. Fill in as many coins as you need for your example:



How much money would you lose in this example? <sum of the coins> cents.

**Part C** (12 points) Fill in the state table corresponding to this state machine.

| S1 | S0 | C1 | C0 | NS1 | NS0 | P | S1 | S0 | C1 | C0 | NS1 | NS0 | P |
|----|----|----|----|-----|-----|---|----|----|----|----|-----|-----|---|
| 0  | 0  | 0  | 1  | 0   | 1   | 0 | 1  | 0  | 0  | 1  | 1   | 1   | 0 |
| 0  | 0  | 1  | 0  | 1   | 0   | 0 | 1  | 0  | 1  | 0  | 1   | 0   | 0 |
| 0  | 0  | 1  | 1  | 0   | 0   | 1 | 1  | 0  | 1  | 1  | 0   | 0   | 0 |
| 0  | 1  | 0  | 1  | 1   | 0   | 0 | 1  | 1  | 0  | 1  | 1   | 1   | 0 |
| 0  | 1  | 1  | 0  | 1   | 1   | 0 | 1  | 1  | 1  | 0  | 0   | 0   | 1 |
| 0  | 1  | 1  | 1  | 0   | 1   | 0 | 1  | 1  | 1  | 1  | 1   | 1   | 0 |