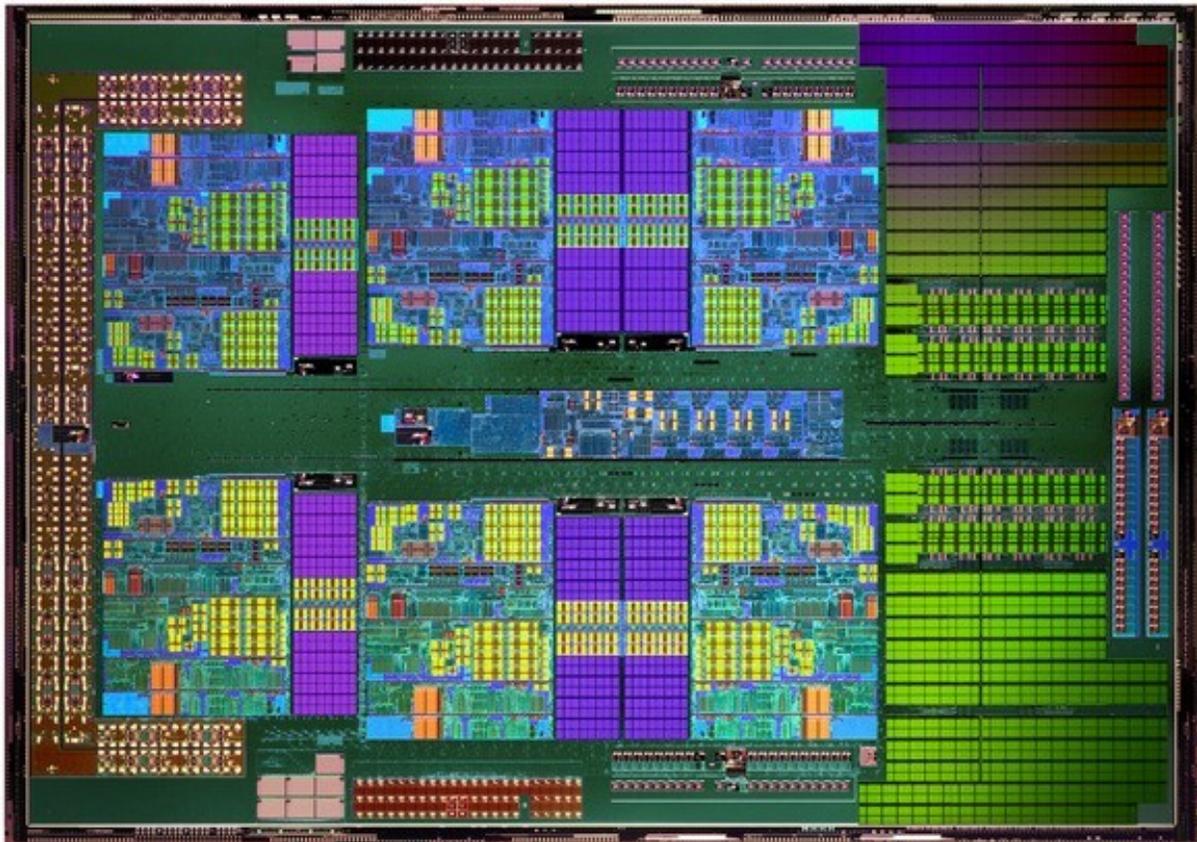


*Instructions:* This is a closed book, closed note exam. Calculators and other electronics are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.  
*Good Luck!*

Your Name (*please print*) \_\_\_\_\_

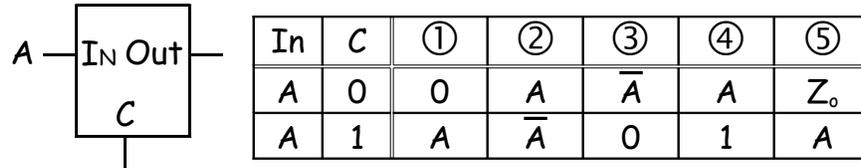
1	2	3	4	5	total
21	32	34	38	30	155



Problem 1 (3 parts, 21 points)

“A chip off the old block”

Part A (15 points) Consider the five definitions for the block drawn below. One block input is the logical value  $A$ . The other input is the control value  $C$ . The output behavior for each of the five definitions is given in the table. Complete the full truth table and state the *logical (gate) names* for each definition. (hint: the first block one appears to mask  $A$  when its control input is low.)



In	C	①	②	③	④	⑤
0	0					
1	0					
0	1					
1	1					

①

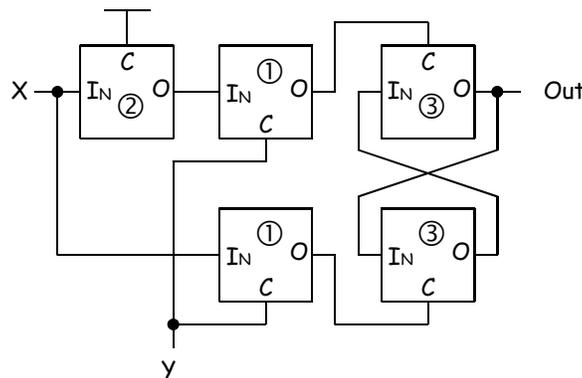
②

③

④

⑤

Part B (6 points) The circuit below is built using these blocks. Describe its behavior. Also give the circuits common name.



X	Y	Out
0	0	
1	0	
0	1	
1	1	

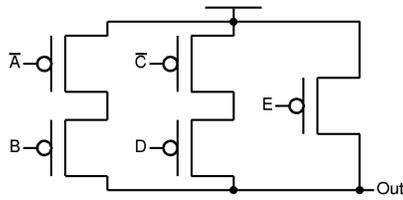
It's a \_\_\_\_\_

Problem 2 (4 parts, 32 points)

Design Fun

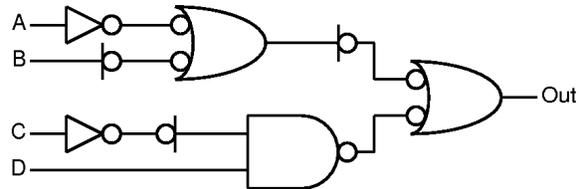
Complete each design below. Be sure to label all signals.

Part A: Complete the following CMOS design. Also express its behavior.



Out = \_\_\_\_\_

Part B: Derive the proper mixed logic expression for the following design. Determine # of switches needed.

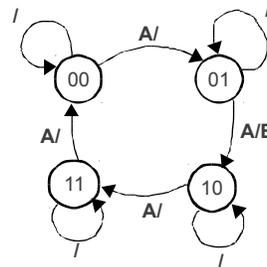


Out = \_\_\_\_\_  
# switches = \_\_\_\_\_

Part C: Implement a toggle cell using required latches and basics gates (including XORs). Also complete the behavior table.

TE	$\overline{\text{CLR}}$	CLK	Out
		$\uparrow\downarrow$	
		$\uparrow\downarrow$	
		$\uparrow\downarrow$	

Part D: Draw the state table for the following state diagram.



A	$S_1$	$S_0$	$NS_1$	$NS_0$	B
0	0	0			
1	0	0			
0	0	1			
1	0	1			
0	1	0			
1	1	0			
0	1	1			
1	1	1			

Problem 3 (3 parts, 34 points)

Memory and Maps

Part A (12 points) Consider a gigabit DRAM chip organized as **64 million addresses** of **16 bit words**. Assume both the DRAM cell and the DRAM chip is square. The column number and offset concatenate to form the memory address. Using the organization approach discussed in class, answer the following questions about the chip. **Express all answers in decimal.**

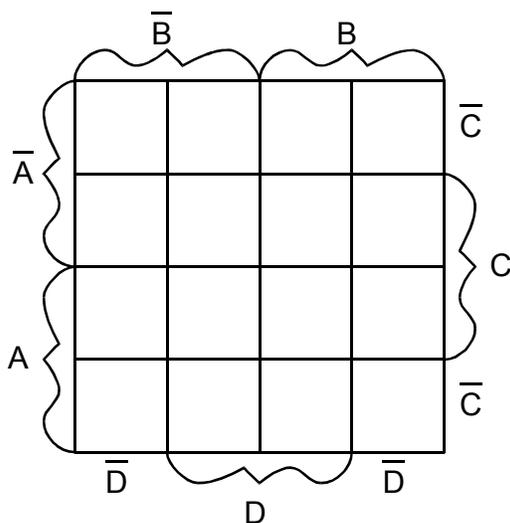
- number of columns \_\_\_\_\_
- column decoder required ( $n$  to  $m$ ) \_\_\_\_\_
- type of mux required ( $n$  to  $m$ ) \_\_\_\_\_
- number of muxes required \_\_\_\_\_
- number of address lines in column number \_\_\_\_\_
- number of address lines in column offset \_\_\_\_\_

Part B (10 points) Consider a memory system with **512 million addresses** of **four byte words** using DRAM chips organized as **64 million addresses** by **16 bit words**

- word** address lines for memory system \_\_\_\_\_
- chips needed in one bank \_\_\_\_\_
- banks for memory system \_\_\_\_\_
- memory decoder required ( $n$  to  $m$ ) \_\_\_\_\_
- DRAM chips required \_\_\_\_\_

Part C (12 points) For the follow expression, derive a simplified **sum of products** expression using a Karnaugh Map. Circle and list **all** prime implicants, indicating which are essential.

$$Out = (\bar{A} \cdot B \cdot \bar{D}) + (A \cdot C \cdot \bar{D}) + (A \cdot B \cdot \bar{C}) + (A \cdot C \cdot D)$$



prime implicants	essential?	
	yes	no
_____	<input type="checkbox"/>	<input type="checkbox"/>
_____	<input type="checkbox"/>	<input type="checkbox"/>
_____	<input type="checkbox"/>	<input type="checkbox"/>
_____	<input type="checkbox"/>	<input type="checkbox"/>
_____	<input type="checkbox"/>	<input type="checkbox"/>
_____	<input type="checkbox"/>	<input type="checkbox"/>
_____	<input type="checkbox"/>	<input type="checkbox"/>
_____	<input type="checkbox"/>	<input type="checkbox"/>

simplified SOP expression \_\_\_\_\_

Problem 4 (4 parts, 38 points)

Number Systems

Part A (8 points) Convert the following notations:

binary notation	decimal notation
1010 1011.1010	
	41.875
binary notation	hexadecimal notation
11 1100 0011.1100 0011 11	
	3F.23

Part B (9 points) For the representations below, determine the most positive value and the step size (difference between sequential values). All answers should be expressed in decimal notation. Fractions (e.g., 3/16ths) may be used. Signed representations are two's complement.

representation	most positive value	step size
signed integer (20 bits) . (0 bits)		
unsigned fixed-point (15 bits) . (5 bits)		
signed fixed-point (10 bits) . (10 bits)		

Part C (9 points) A 20 bit floating point representation has a 13 bit mantissa field, a 6 bit exponent field, and one sign bit. *Express all answers in decimal.*

What is the largest value that can be represented (closest to infinity)?

\_\_\_\_\_

What is the smallest value that can be represented (closest to zero)?

\_\_\_\_\_

How many decimal significant figures are supported?

\_\_\_\_\_

Part D (12 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a **five bit unsigned fixed-point** and **five bit two's complement fixed-point** representations.

$$\begin{array}{r}
 1111.0 \\
 + \quad 1.1 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 10.00 \\
 + 10.00 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 10001 \\
 - \quad 11 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 1.1100 \\
 - 0.1011 \\
 \hline
 \end{array}$$

result

unsigned error?	<input type="checkbox"/> no <input type="checkbox"/> yes			
signed error?	<input type="checkbox"/> no <input type="checkbox"/> yes			

Problem 5 (1 part, 30 points)

Assembly Programming

**Part A** (30 points) Complete an assembly language routine that computes the **average of positives integers** in a **200** element array. The array begins at array 5000. Ignore integers in the array that negative (less than zero). Remember that memory is byte addressed and each word in memory is four bytes long (the first word starts at 5000, the second word starts at 5004, etc.) Each time a positive integer is encountered, the number of positive integers (\$5) is incremented. Later \$5 is used to compute the average. Use the following register assignments: \$1= array pointer, \$2= end address, \$3= current element, \$4= current sum, \$5= num positive integers, \$6= branch predicate. The result (positive integer average) should be stored in \$4.

<i>label</i>	<i>instruction</i>	<i>comment</i>
<b>PosAvg:</b>		# init array ptr
		# compute end address
		# clear current sum
		# clear number pos ints
		# load current element
		# if element < 0
		# then skip
		# else add to sum
		# increment num pos ints
		# move to next element
		# if not done, loop
		# sum / num pos ints
		# move avg to \$4
	jr \$31	# return to caller

MIPS Instruction Set

<i>instruction</i>	<i>example</i>	<i>meaning</i>
<b>arithmetic</b>		
add	add \$1,\$2,\$3	$S1 = S2 + S3$
subtract	sub \$1,\$2,\$3	$S1 = S2 - S3$
add immediate	addi \$1,\$2,100	$S1 = S2 + 100$
add unsigned	addu \$1,\$2,\$3	$S1 = S2 + S3$
subtract unsigned	subu \$1,\$2,\$3	$S1 = S2 - S3$
add immediate unsigned	addiu \$1,\$2,100	$S1 = S2 + 100$
set if less than	slt \$1, \$2, \$3	if ( $S2 < S3$ ), $S1 = 1$ else $S1 = 0$
set if less than immediate	slti \$1, \$2, 100	if ( $S2 < 100$ ), $S1 = 1$ else $S1 = 0$
set if less than unsigned	sltu \$1, \$2, \$3	if ( $S2 < S3$ ), $S1 = 1$ else $S1 = 0$
set if < immediate unsigned	sltui \$1, \$2, 100	if ( $S2 < 100$ ), $S1 = 1$ else $S1 = 0$
multiply	mult \$2,\$3	Hi, Lo = $S2 * S3$ , 64-bit signed product
multiply unsigned	multu \$2,\$3	Hi, Lo = $S2 * S3$ , 64-bit unsigned product
divide	div \$2,\$3	Lo = $S2 / S3$ , Hi = $S2 \bmod S3$
divide unsigned	divu \$2,\$3	Lo = $S2 / S3$ , Hi = $S2 \bmod S3$ , unsigned
<b>transfer</b>		
move from Hi	mfhi \$1	$S1 = Hi$
move from Lo	mflo \$1	$S1 = Lo$
load upper immediate	lui \$1,100	$S1 = 100 \times 2^{16}$
<b>logic</b>		
and	and \$1,\$2,\$3	$S1 = S2 \& S3$
or	or \$1,\$2,\$3	$S1 = S2   S3$
and immediate	andi \$1,\$2,100	$S1 = S2 \& 100$
or immediate	ori \$1,\$2,100	$S1 = S2   100$
nor	nor \$1,\$2,\$3	$S1 = \text{not}(S2   S3)$
xor	xor \$1, \$2, \$3	$S1 = S2 \oplus S3$
xor immediate	xori \$1, \$2, 255	$S1 = S2 \oplus 255$
<b>shift</b>		
shift left logical	sll \$1,\$2,5	$S1 = S2 \ll 5$ (logical)
shift left logical variable	sllv \$1,\$2,\$3	$S1 = S2 \ll S3$ (logical), variable shift amt
shift right logical	srl \$1,\$2,5	$S1 = S2 \gg 5$ (logical)
shift right logical variable	srlv \$1,\$2,\$3	$S1 = S2 \gg S3$ (logical), variable shift amt
shift right arithmetic	sra \$1,\$2,5	$S1 = S2 \gg 5$ (arithmetic)
shift right arithmetic variable	srav \$1,\$2,\$3	$S1 = S2 \gg S3$ (arithmetic), variable shift amt
<b>memory</b>		
load word	lw \$1, 1000(\$2)	$S1 = \text{memory}[S2+1000]$
store word	sw \$1, 1000(\$2)	$\text{memory}[S2+1000] = S1$
load byte	lb \$1, 1002(\$2)	$S1 = \text{memory}[S2+1002]$ in least sig. byte
load byte unsigned	lbu \$1, 1002(\$2)	$S1 = \text{memory}[S2+1002]$ in least sig. byte
store byte	sb \$1, 1002(\$2)	$\text{memory}[S2+1002] = S1$ (byte modified only)
<b>branch</b>		
branch if equal	beq \$1,\$2,100	if ( $S1 = S2$ ), $PC = PC + 4 + (100*4)$
branch if not equal	bne \$1,\$2,100	if ( $S1 \neq S2$ ), $PC = PC + 4 + (100*4)$
<b>jump</b>		
jump	j 10000	$PC = 10000*4$
jump register	jr \$31	$PC = S31$
jump and link	jal 10000	$S31 = PC + 4$ ; $PC = 10000*4$