

Instructions: This is a closed book, closed note exam. Calculators are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.
Good Luck!

Your Name (*please print*) _____

1	2	3	4	total
<input type="text"/>				
18	32	28	22	100



Problem 1 (2 parts, 18 points)

Datapath Elements

Part A (9 points) Consider the following inputs, shift types, and directions. Determine the resulting outs (in hexadecimal).

Input Value	Output Value	Shift Type	Shift Amount
0x87654321		rotate	left 8 bits
0x87654321		arithmetic	right 12 bits
0x87654321		logical	left 28 bits

Part B (9 points) Consider the following input and logical operation function codes. Determine the *logical function* and output value (in hexadecimal) for the operation.

X Input	Y Input	Output Value	Logical Function	Function Code
87654321	00FF00FF			E
87654321	00FF00FF			3
87654321	00FF00FF			7

Problem 2 (3 parts, 32 points)

Memory Systems

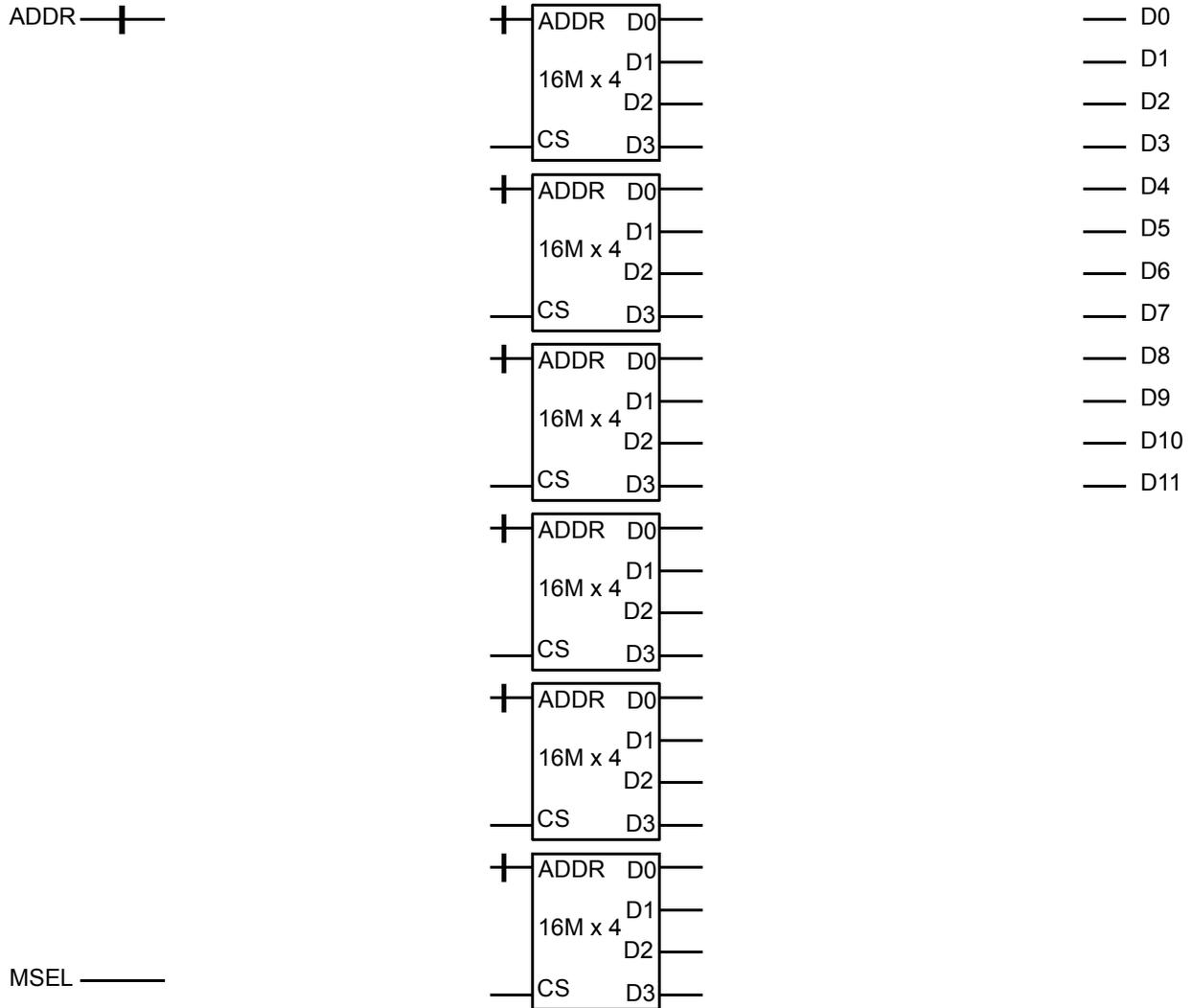
Part A (12 points) Consider a DRAM chip organized as **512 million addresses** of **eight bit words**. Assume both the DRAM cell and the DRAM chip is square. The column number and offset concatenate to form the memory address. Using the organization approach discussed in class, answer the following questions about the chip. **Express all answers in decimal.**

- number of columns _____
- column decoder required (n to m) _____
- type of mux required (n to m) _____
- number of muxes required _____
- number of address lines in column number _____
- number of address lines in column offset _____

Part B (10 points) Consider a **eight Gbyte** memory system with **two billion addresses** of **four byte words** using DRAM chips organized as **512 million addresses** by **eight bit words**.

- word** address lines for memory system _____
- chips needed in one bank _____
- banks for memory system _____
- memory decoder required (n to m) _____
- DRAM chips required _____

Part C (10 points) Design a 48 M address x 8 bit memory system with six 16 M address x 4 bit memory chips. **Label all busses and indicate bit width.** Assume R/W is connected and not shown here. Use a decoder if necessary. Place a star on the chip(s) that contain address 25,000,000.



Problem 3 (5 parts, 28 points)

Microcode

Using the supplied datapath, write microcode fragments to accomplish the following procedures. Express all values in hexadecimal notation. Use ‘X’ when a value is don’t cared. For shift operations, expression shift amount as unsigned value. The shift direction field (*dir*) is 1 for left shifts, 0 for right shifts. For maximum credit, complete the description field.

Part A (5 points) $\$7 \leftarrow \$8 + \$9$. Use only registers 7, 8, and 9.

#	X	Y	Z	rwe	im en	im va	au en	-a /s	lu en	lf	su en	st	dir	description
1														

Part B (5 points) Mask all but the ten least significant bits of \$6. Use only register 6.

#	X	Y	Z	rwe	im en	im va	au en	-a /s	lu en	lf	su en	st	dir	description
1														

Part C (5 points) Rotate register \$3 by 16 bits. Use only register 3.

#	X	Y	Z	rwe	im en	im va	au en	-a /s	lu en	lf	su en	st	dir	description
1														

Part D (8 points) $\$5 \leftarrow 63 * \4 . Use only registers 4 and 5.

#	X	Y	Z	rwe	im en	im va	au en	-a /s	lu en	lf	su en	st	dir	description
1														
2														

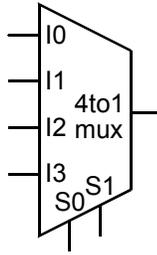
Part E (5 points) $\$7 \leftarrow \$5 \text{ xor } \$6$. Use only registers 5, 6, and 7.

#	X	Y	Z	rwe	im en	im va	au en	-a /s	lu en	lf	su en	st	dir	description
1														

Problem 4 (2 parts, 22 points)

Toggle Cells and Counters

Part A (11 points) Design a toggle cell using **two transparent latches**, **one 4to1 mux**, and **one inverter** (use icons, **labeling inputs & outputs**). Your toggle cell should have an active high toggle enable input **TE**, and an active low clear input **CLR**, clock inputs Φ_1 and Φ_2 , and an output **Out**. The **CLR** signal has precedence over **TE**. Also complete the behavior table for the toggle cell.

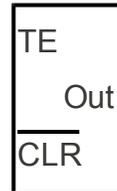


	TE	$\overline{\text{CLR}}$	CLK	Out
— Out	0	0	$\uparrow\downarrow$	
	1	0	$\uparrow\downarrow$	
	0	1	$\uparrow\downarrow$	
	1	1	$\uparrow\downarrow$	

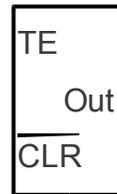


Part B (11 points) Now combine these toggle cells to build a **divide by 7** counter. Your counter should have an external clear, external count enable, and three count outputs O_2 , O_1 , O_0 . Use any basic gates (AND, OR, NAND, NOR, & NOT) you require. Assume clock inputs to the toggle cells are already connected. *Your design should support multi-digit systems.*

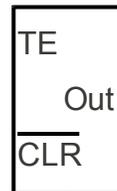
Ext CE —



— O_0



— O_1



— O_2

Ext CLR —