Instructions: This is a closed book, closed note exam. Calculators are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.
Good Luck!

Your Name (***please print***) ____

1	2	3	4	total
30	25	30	15	100

Problem 1 (3 parts, 30 points) Memory Systems

Part A (10 points) Consider a **256 Mbit** DRAM chip organized as **32 million addresses** of **one byte words**. Assume both the DRAM cell and the DRAM chip is square. The column number and offset concatenate to form the memory address. Using the organization approach discussed in class, answer the following questions about the chip. **Express all answers in decimal**.

number of columns ____________________

column decoder required (*n* to *m*) ____________________

type of mux required (*n* to *m*) ____________________

number of muxes required ____________________

number of address lines in column number ____________________

number of address lines in column offset ____________________

Part B (10 points) Consider a **one Gbyte** memory system with **128 million addresses** of **eight byte words** using DRAM chips organized as **16 million** addresses by **16 bit words.**

word address lines for memory system ____________________

chips needed in one bank ____________________

banks for memory system ____________________

memory decoder required (*n* to *m*) ____________________

DRAM chips required ____________________

Part C (10 points) (10 points) Design a 96M address x 4 bit memory system using 32M address x 4 bit memory chips. **Label all busses and indicate bit width**. Assume R/W is connected and not shown here. Use a decoder if necessary. Be sure to include the address bus, data bus, and MSEL.

Problem 2 (3 parts, 25 points) Microcode

Using the supplied datapath, write microcode fragments to accomplish the following procedures. Express all values in hexadecimal notation. Use 'X' when a value is don't cared. For maximum credit, complete the description field. ∩ means bitwise logical AND.

Part A (10 points) **Use only registers 1 & 2.**

$$R_2 = \frac{\frac{R_1}{256} + R_1 \cap 255}{2}$$

#	*X*	*Y*	*Z*	*rwe*	*im en*	*im va*	*au en*	*-a /s*	*lu en*	*lf*	*su en*	*st*	*ld en*	*st en*	*r/ -w*	*msel*	*description*
1																	
2																	
3																	
4																	

Part B (10 points) mem[0x100] = 0 - mem[0x100]. **Use only registers 1, 2, & 3.**

#	*X*	*Y*	*Z*	*rwe*	*im en*	*im va*	*au en*	*-a /s*	*lu en*	*lf*	*su en*	*st*	*ld en*	*st en*	*r/ -w*	*msel*	*description*
1																	
2																	
3																	
4																	
5																	

Part C (5 points) Exchange R_1 and R_2. **Use only registers 1, 2 & 3.**

#	*X*	*Y*	*Z*	*rwe*	*im en*	*im va*	*au en*	*-a /s*	*lu en*	*lf*	*su en*	*st*	*ld en*	*st en*	*r/ -w*	*msel*	*description*
1																	
2																	
3																	

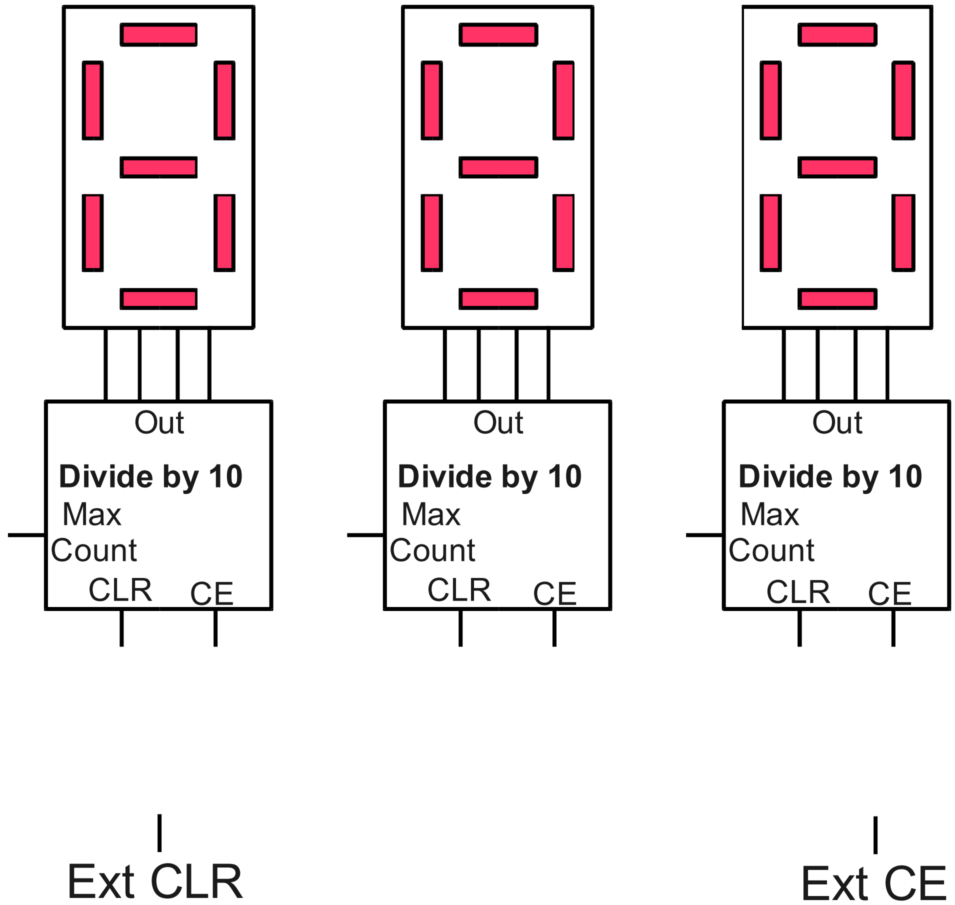
Problem 3 (3 parts, 30 points) — Counters

Part A (10 points) Design a toggle cell using transparent latches and basic gates. Use an icon for the latch. Your toggle cell should have an active high toggle enable input **TE**, and an active low clear input $\overline{\textbf{CLR}}$, clock inputs Φ_1 and Φ_2, and an output **Out**. The $\overline{\textbf{CLR}}$ signal has precedence over **TE**. Label all signals. Also complete the behavior table for the toggle cell.

TE	$\overline{CLR}$	CLK	Out
0	0	↑↓	
1	0	↑↓	
0	1	↑↓	
1	1	↑↓	

Part B (10 points) Now combine these toggle cells to build a **divide by 10** (decade) counter. Your counter should have an external clear, external count enable, and four count outputs O_3, O_2, O_1, O_0. Use any basic gates (AND, OR, NAND, NOR, & NOT) you require. Assume clock inputs to the toggle cells are already connected. *Your design should support multi-digit systems*.

Part C (10 points) Build a three digit decimal counter (0 - 999) using three decade counters drawn below. Use any basic gates you require. Assume clock inputs are already connected.



Problem 4 (2 parts, 15 points) Microcode

Part A (9 points) Consider the following input and output values for a shift operation. Determine the shift *type* and *amount* required to achieve the listed transformation. I/Os are in hexadecimal.

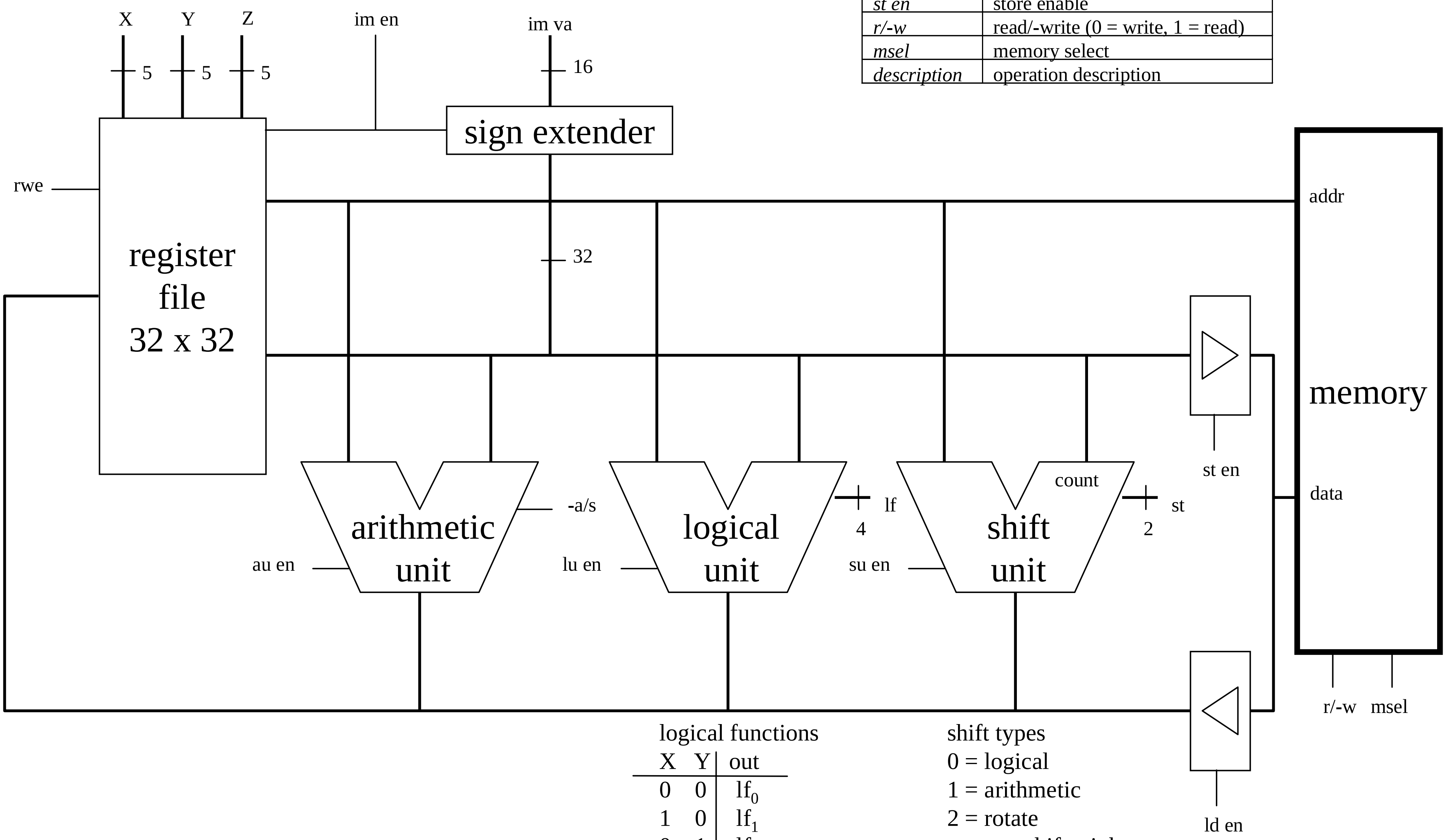
Input Value	Output Value	Shift Type	Shift Amount (signed decimal value)
87654321	32187654		
87654321	54321000		
87654321	FFFFFF87		

Part B (6 points) Consider the following input and output values for a logical operation. Determine the *logical function* and *function code* (in hexadecimal) required for the operation.

X Input	Y Input	Output	Logical Function	Function Code
87654321	0000FFFF	0000FFFF		
87654321	0000FFFF	FFFFBCDE		

cycle	cycle number
X	register driven onto X bus
Y	register driven onto Y bus
Z	register written from Z bus
rwe	register write enable
im en	immediate enable on Y bus
im va	immediate value

au en	arithmetic unit enable
-a/s	-add / sub (0 = add, 1 = subtract)
lu en	logical unit enable
lf	logical function
su en	shift unit enable
st	shift type
ld en	load enable
st en	store enable
r/-w	read/-write (0 = write, 1 = read)
msel	memory select
description	operation description



logical functions

X	Y	out
0	0	lf_0
1	0	lf_1
0	1	lf_2
1	1	lf_3

shift types
0 = logical
1 = arithmetic
2 = rotate
+ count shifts right
- count shifts left