

*Instructions:* This is a closed book, closed note exam. Calculators are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.

*Good Luck!*

Your Name (*please print*) \_\_\_\_\_

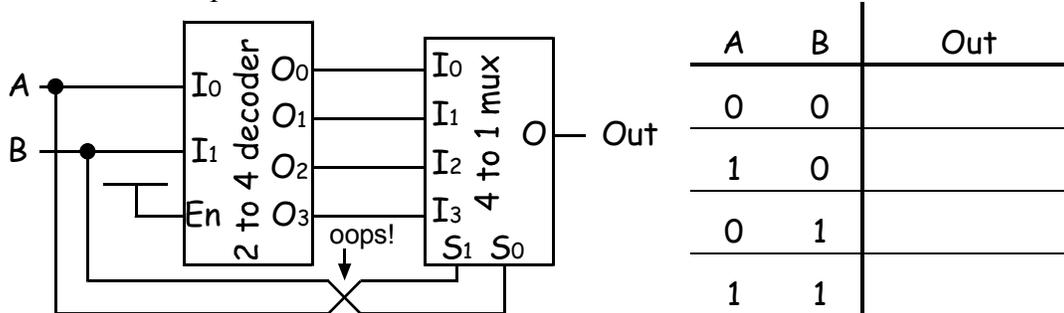
1	2	3	4	total
<input type="text"/>				
24	28	24	24	100



Problem 1 (4 parts, 24 points)

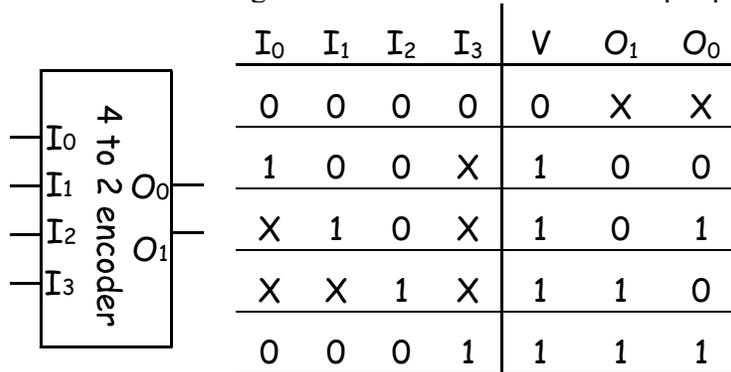
Building Blocks

Part A (8 points) Consider the circuit below. Complete the truth table. Then state what logical function this circuit implements.



This wacky circuit is \_\_\_\_\_

Part B (6 points) Consider the following circuit below. Determine its input priority.

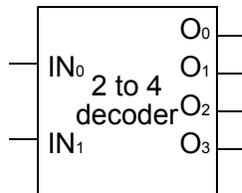


\_\_\_\_\_ > \_\_\_\_\_ > \_\_\_\_\_ > \_\_\_\_\_

Part C (4 points) Derive a simplified expression for O<sub>1</sub>.

O<sub>1</sub> = \_\_\_\_\_

Part D (6 points) Implement a 2-input NAND using a 2-to-4 decoder and a single OR gate (which may have any number of inputs). Label the inputs **A** and **B**, and output **A NAND B**.



Problem 2 (3 parts, 28 points)

Number Systems

Part A (10 points) Convert the following notations:

binary notation	decimal notation
1100 1010.	
1010 0100.1000 1	
111 1100.11	
octal notation	hexadecimal notation
4733.6	
24.32	

Part B (12 points) For the 16 bit representations below, determine the most positive value and the step size (difference between sequential values). **All answers should be expressed in decimal notation.** Fractions (e.g., 3/16ths) may be used. Signed representations are two's complement.

representation	most positive value	step size
unsigned integer (16 bits) . (0 bits)		
signed fixed-point (11 bits) . (5 bits)		
signed fixed-point (9 bits) . (7 bits)		
signed fixed-point (14 bits) . (2 bits)		

Part C (6 points) A 34 bit floating point representation has a 24 bit mantissa field, a 9 bit exponent field, and one sign bit.

What is the largest value that can be represented (closest to infinity)?      2 \_\_\_\_\_

What is the smallest value that can be represented (closest to zero)?      2 \_\_\_\_\_

How many decimal significant figures are supported?      \_\_\_\_\_

Problem 3 (3 parts, 24 points)

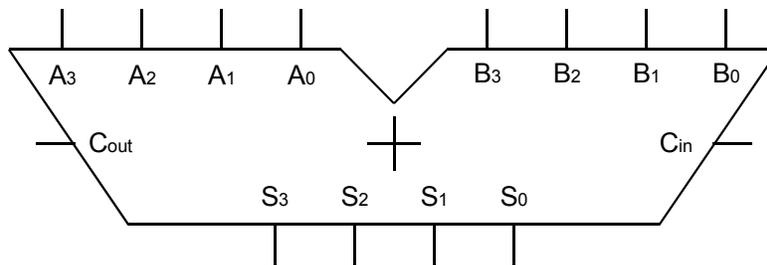
“Go Figure”

Part A (12 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a **six bit unsigned fixed-point** and **six bit two’s complement fixed-point** representations.

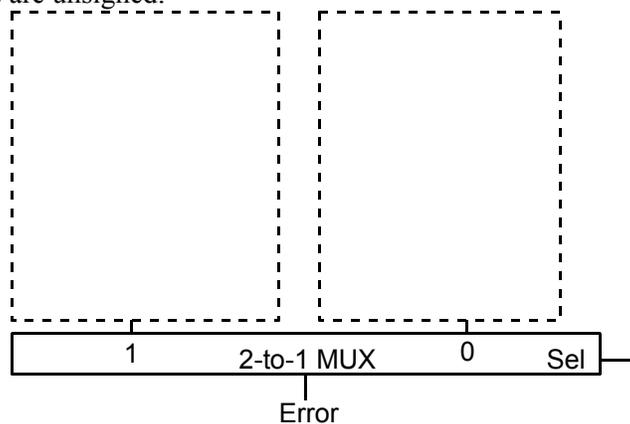
$$\begin{array}{r}
 111.101 \\
 + 011.100 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 1.010 \\
 + 101.011 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 101.011 \\
 - 10.110 \\
 \hline
 \end{array}
 \qquad
 \begin{array}{r}
 1.010 \\
 - 101.011 \\
 \hline
 \end{array}$$

result
unsigned error?
signed error?

Part B (6 points) The adder below adds two four bit numbers A and B and produces a four bit result S. Add extra digital logic to support subtraction as well as addition. Label inputs  $X_3, X_2, X_1, X_0, Y_3, Y_2, Y_1, Y_0, \overline{ADD/SUB}$  and outputs  $Z_3, Z_2, Z_1, Z_0$ .



Part C (6 points) Below is a partial implementation of an overflow error detector for the adder/subtractor in part B. It detects errors in addition or subtraction of signed and unsigned numbers. Complete the implementation by filling in the dashed boxes with the appropriate error detector circuitry. For full credit, label all the inputs using signals from **part B** (e.g.,  $\overline{ADD/SUB}$  and  $S_3$ ) and the additional input signal  $\overline{Unsigned/Signed}$  which is 1 if the numbers being added/subtracted are two’s complement numbers and which is 0 if the numbers are unsigned.



Problem 4 (3 parts, 24 points)

Registers and Latches

Part A (8 points) Implement a transparent latch using only inverters and pass gates. Label the inputs **In** and **En**, and output **Out**.

Part B (10 points) Implement a register below using needed muxes, latches, pass gates, and inverters (all in icon form). Complete the behavior table at right. Recall that the CLK signal indicates a full  $\Phi_1$   $\Phi_2$  cycle; so the output should be the value at the end of a cycle (with the given inputs).

In	WE	RE	Clk	Out
A	0	0	↑↓	
A	1	0	↑↓	
A	0	1	↑↓	
A	1	1	↑↓	

In —

— Out



Part C (6 points) Assume the following signals are applied to your register. Draw the output signal **Out**. Draw a vertical line where **In** is sampled. Assume **Out** is initially zero.

