

ECE2020 A Fall 2021 Test 1

Name: _____

- Only a writing implement may be used on this exam (i.e. no notes or electronics).
- This test is 50 minutes.
- Partial credit can only be awarded for work shown.

Honor pledge:

On my honor, I pledge that I will neither receive nor provide improper assistance in the completion of this test. I understand and accept my responsibility as a member of the Georgia Tech Community to uphold the Honor Code at all times, and I know that I have options for reporting honor violations at osi.gatech.edu.

GTID: _____

Signature: _____

Boolean Identities

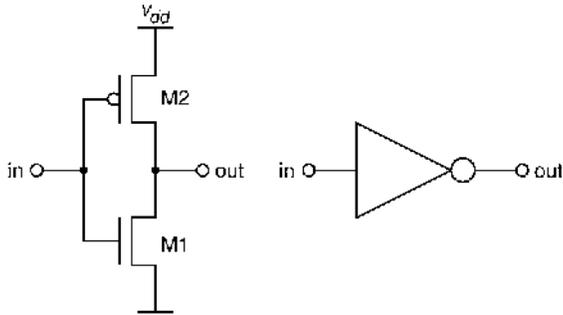
Identity	$A + 0 = A$	$A \cdot 1 = A$
Dominance	$A + 1 = 1$	$A \cdot 0 = 0$
Idempotence	$A + A = A$	$A \cdot A = A$
Inverse	$A + \bar{A} = 1$	$A \cdot \bar{A} = 0$
Commutative	$A + B = B + A$	$A \cdot B = B \cdot A$
Associative	$A + (B + C) = (A + B) + C$	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$
Distributive	$A \cdot (B + C) = A \cdot B + A \cdot C$	$A + B \cdot C = (A + B) \cdot (A + C)$
Absorption	$A \cdot (A + B) = A$	$A + A \cdot B = A$
DeMorgan's	$\overline{(A + B)} = \bar{A} \cdot \bar{B}$	$\overline{(A \cdot B)} = \bar{A} + \bar{B}$
Double Complement	$\bar{\bar{A}} = A$	
FOIL	$(A + B) \cdot (C + D) = A \cdot C + A \cdot D + B \cdot C + B \cdot D$	
Disappearing opposite	$A + \bar{A} \cdot B = A + B$	

Select definitions

Prime implicant: an implicant that is as large as possible.

Essential prime implicant: a prime implicant that covers a minterm that no other prime implicant covers.

CMOS inverter



This stuff is for scratch work and will not be graded unless you tell me that something on here needs to be graded.

0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

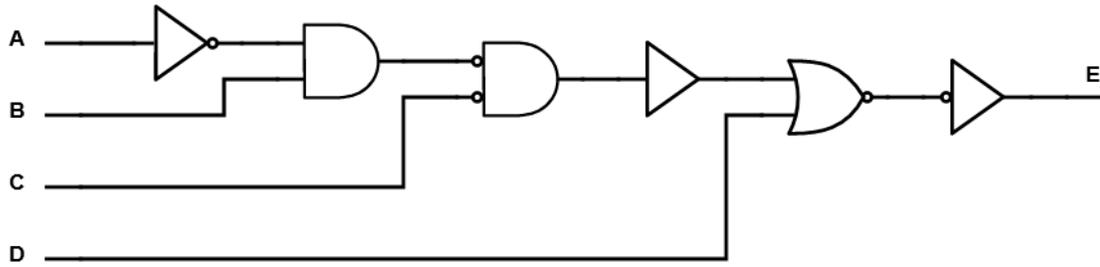
0	0	0	0	
0	0	0	1	
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1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Problem 1 (8+12 points):

a) Write the Boolean expression represented by this gate schematic. Do not simplify or otherwise manipulate anything; the expression should be what is directly represented here.



E = _____

b) Fill in the truth table for the logic in a) above. The table is separated into two sections just to fit better on the page.

A	B	C	D	E
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	

A	B	C	D	E
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Problem 2 (10 points):

Draw a gate schematic that directly implements this Boolean expression (i.e. do not algebraically change anything).

$$G = \overline{\overline{A + B} \cdot B + \overline{C}}$$

Problem 3 (18 points):

Implement the following Boolean expression in proper CMOS (N-FETs and P-FETs). Assume that inputs and their complements are available (i.e. you may use something like \bar{C} as an input to a FET if needed).

$$F = \overline{\overline{\overline{A}} \cdot \overline{\overline{B}} \cdot C}$$

Derive expressions for the pull-up and pull-down switch networks (p.u. and p.d.) here:

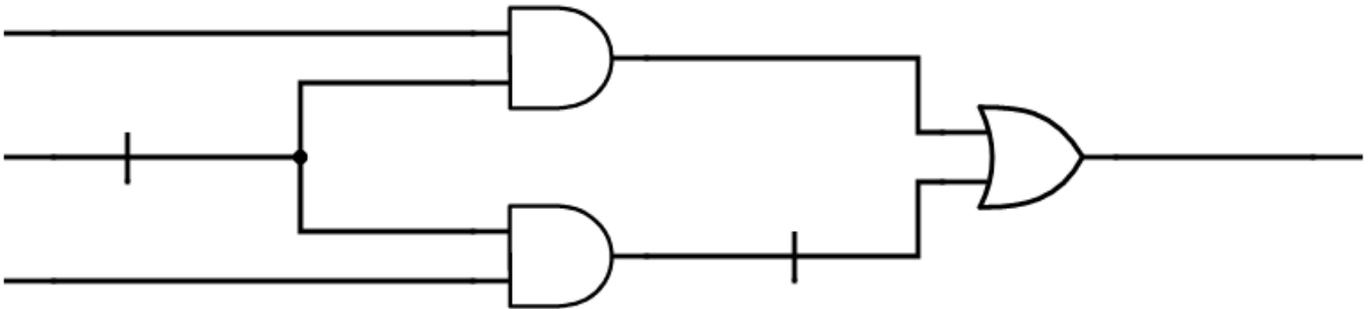
Draw CMOS here:

p.u. = _____

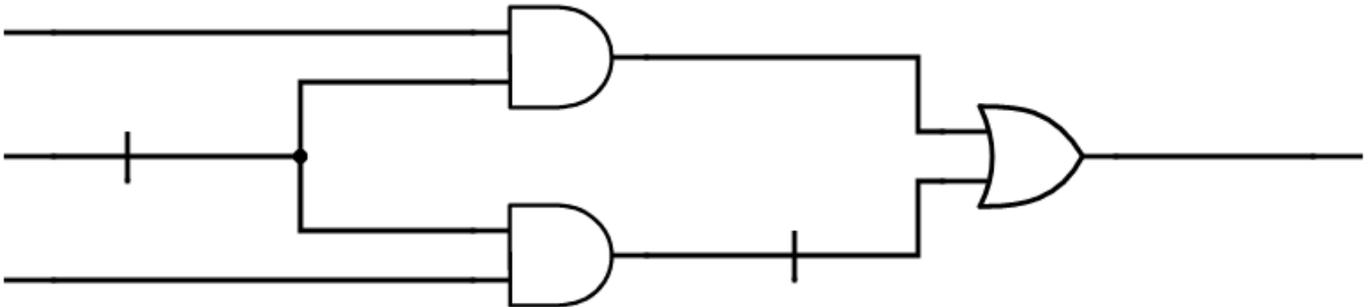
p.d. = _____

Problem 4 (16+4 points):

a) Manipulate the following mixed-logic schematic to implement it using only **NORs** and **inverters**. Minimize the number of inverters.



b) This time, implement it using only **ANDs** and **inverters**. Minimize the number of inverters.



c) If the circuits above (after your manipulations) were built using physical chips, how many of the following types of gates would be required?

Gate type	# needed for a)	# needed for b)
NOT		
AND		
OR		
NAND		
NOR		

Problem 4 (18+4 points):

a) Using the truth table below, create a K-map and solve for a minimal sum-of-products expression.

A	B	C	D	Y
0	0	0	0	X
0	0	0	1	X
0	0	1	0	X
0	0	1	1	X
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	X
1	1	1	1	1

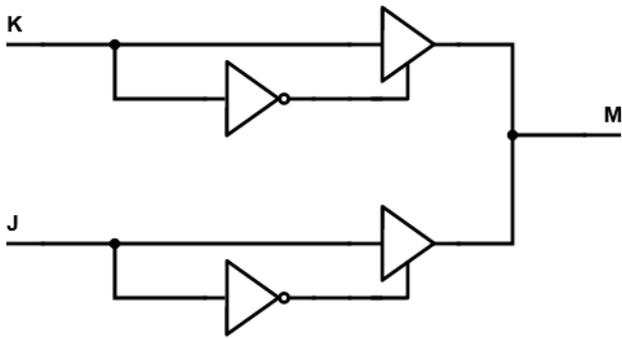
Label the rows and columns of the K-map appropriately.

Y = _____

b) List all of the essential prime implicants in the above K-map:

Problem 5) (10 points)

Complete the truth table for this circuit.



K	J	M
0	0	
0	1	
1	0	
1	1	