

ECE 2020

Digital System Design

Quiz I

September 13, 2012

This exam is closed book and closed note and no calculators.

There are four questions. Do read them over before you start to work. If you need to make any assumptions, state them.

The meaning of each question should be clear, but if something does not make any sense to you, please ask for clarification. If you run out of room, please continue on the back of the previous page.

Good Luck!

Name (Please print) _____

This exam will be conducted according to the Georgia Tech Honor Code. I pledge to neither give nor receive unauthorized assistance on this exam and to abide by all provisions of the Honor Code.

Signed _____

Question	Score	Max
1		20
2		30
3		30
4		20
Total		100

1. (20) Number representations

a) Convert the following unsigned **binary** number to **hexadecimal**

1010 1101 0110 0010 0000 0011 1100 1111 0100 = _____

b) Convert the unsigned 8-bit unsigned **binary** number 10010110 to **decimal**.

c) Convert the **hexadecimal** number 0x34 to **decimal**.

d) Convert this **hexadecimal** number to **binary** (please space in nibbles).

0x4FEEDBAC = _____

2. (30) Gates

a) Design a CMOS (nfet/pfet) implementation of a gate implementing $F = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{D}$ and give both gate symbols for this device. As part of your design process write expressions for both switching functions (f_{sp} and f_{sn}). (Note: There are five (easy) pieces to this answer).

b) Consider the majority (two out of three) function $F = ab + ac + bc = a(b + c) + bc$. Implement the function as a (non-primitive) CMOS gate using a minimum number of transistors. (hint: use the factored form above and you will need one inverter).

3. (30) Suppose $F(A,B,C) = A\bar{B} + \bar{A}C + ABC$.

a) Give a truth table for F.

b) Give its product of maxterm ($\prod(i)$) representation for F.

c) Give a sum of minterms ($m_i + m_j + \dots$) for F.

4. (20) Implement $G = (A + \overline{B}) \cdot (\overline{C \cdot D} + E) \cdot F$ using NAND2, NOR3, and INV gates and assuming **only** active high input signals are available. Correct mixed logic conventions must be observed, and **the function must be implemented exactly as written**. Choose the output sense (active high or low) to minimize inverters.